EXHIBIT 4

US006828195B2

(12) **United States Patent**
Mo et al.

(10) **Patent No.: US 6,828,195 B2**
(45) **Date of Patent: Dec. 7, 2004**

(54) **METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/347,254**

(22) Filed: **Jan. 17, 2003**

(65) **Prior Publication Data**

US 2003/0127688 A1 Jul. 10, 2003

Related U.S. Application Data

(60) Continuation of application No. 09/854,102, filed on May 9, 2001, now Pat. No. 6,521,497, which is a division of application No. 08/970,221, filed on Nov. 14, 1997, now Pat. No. 6,429,481.

(51) **Int. Cl.**[7] **H01L 21/336**

(52) **U.S. Cl.** **438/270**; 438/589

(58) **Field of Search** 438/270–272, 438/589

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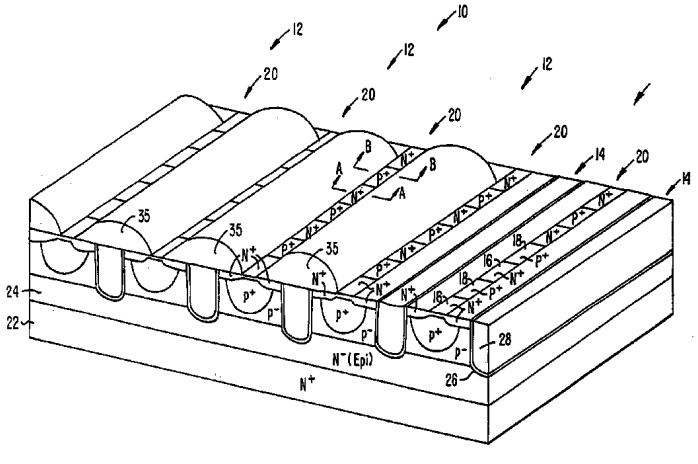
(57) **ABSTRACT**

A trenched field effect transistor is provided that includes (a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

23 Claims, 9 Drawing Sheets



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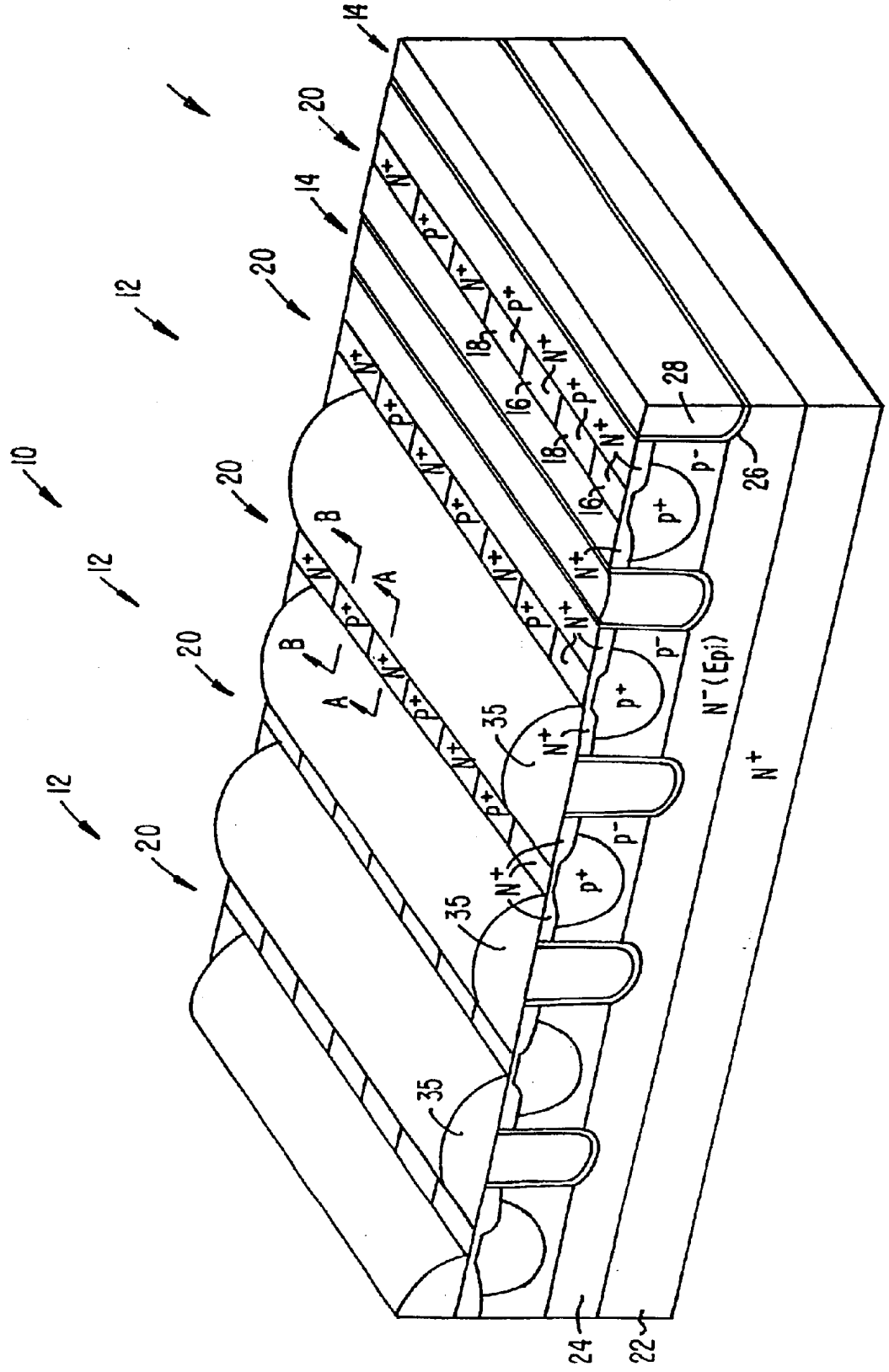
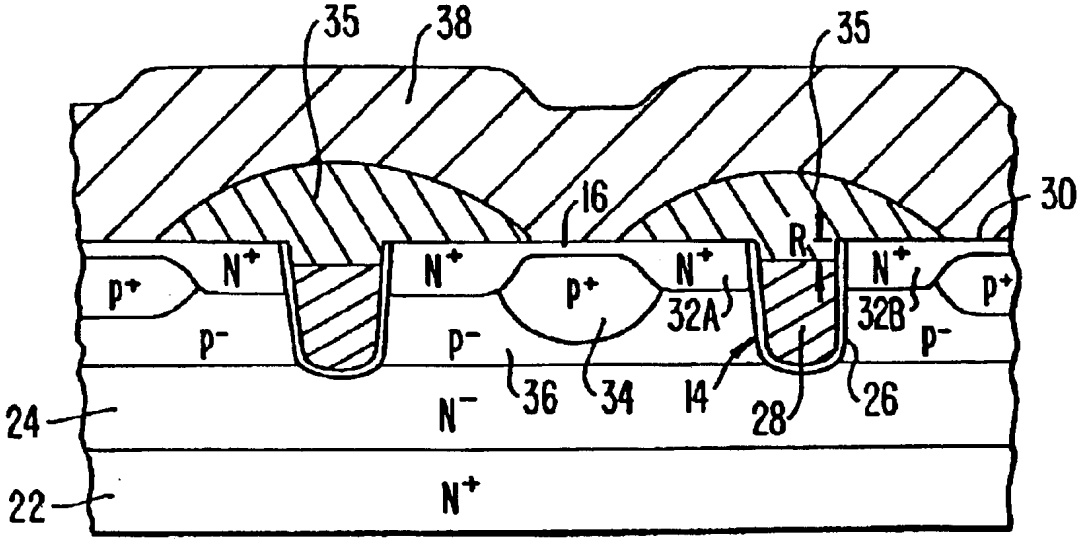


FIG. 1.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N+
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36
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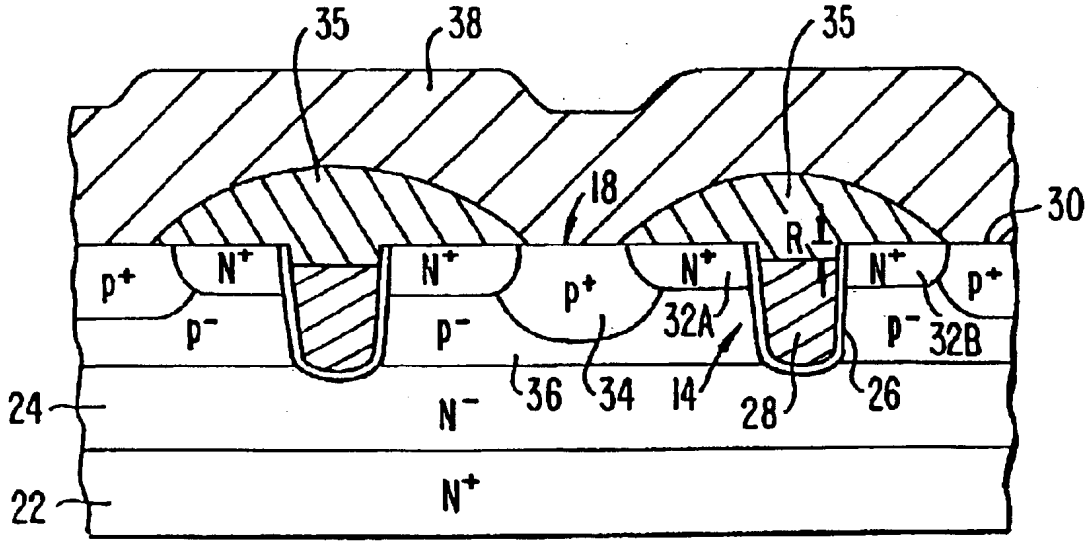
26
24
N-
22
N+

FIG. 1A.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22
N+

FIG. 1B.

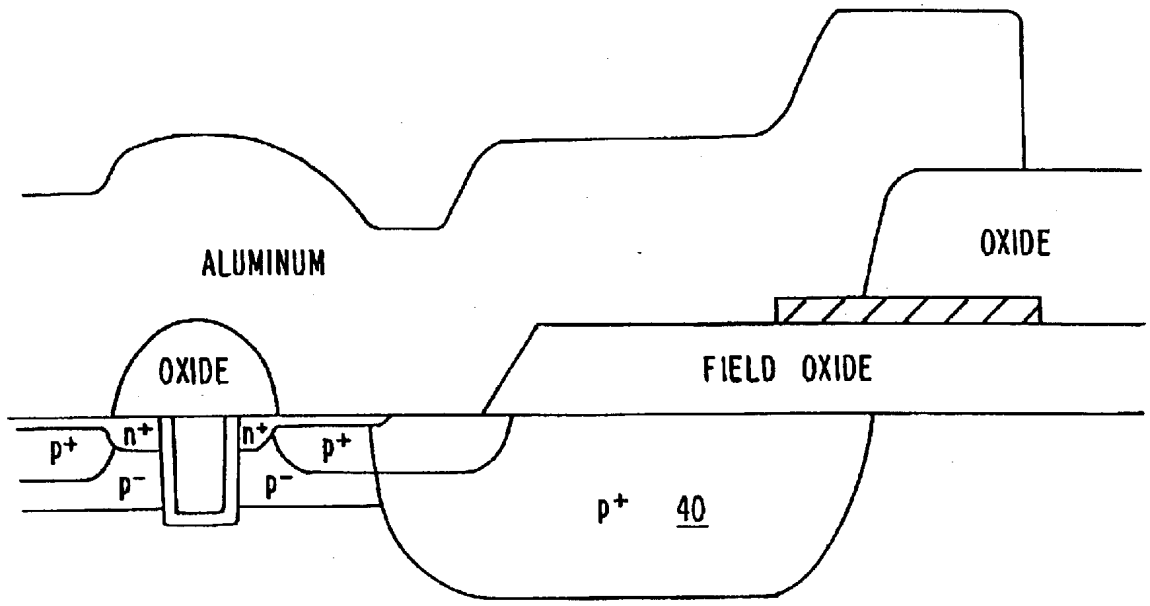


FIG. 2.

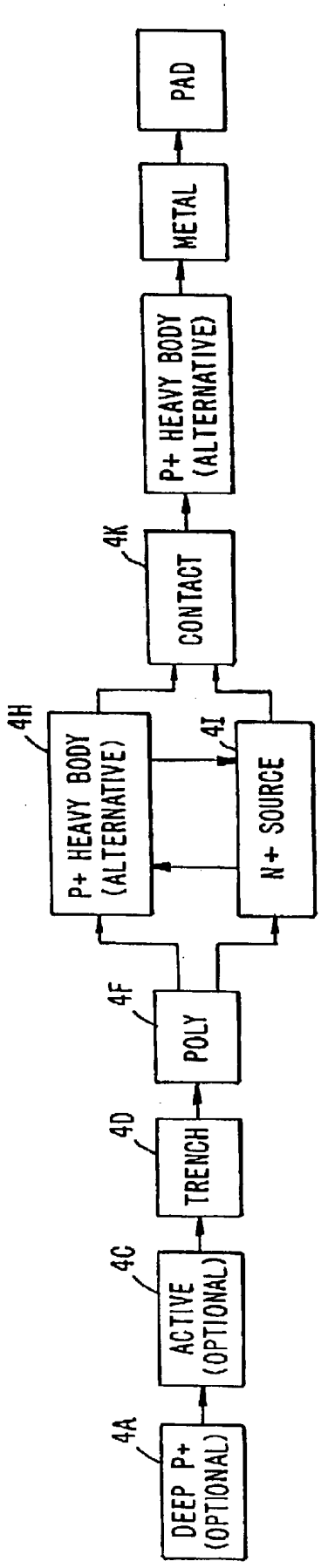
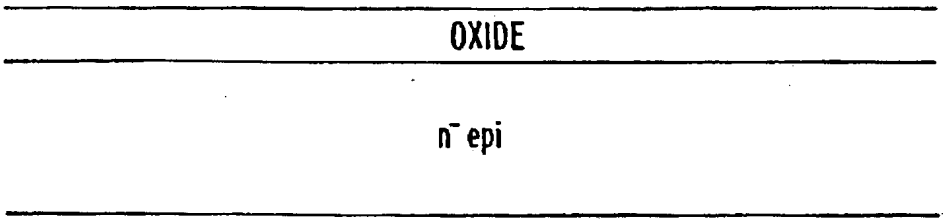

PAD
METAL
P+ HEAVY BODY (ALTERNATIVE)
4K
CONTACT
4H
P+ HEAVY BODY (ALTERNATIVE)
4I
N+ SOURCE
4F
POLY
4D
TRENCH
4C
ACTIVE (OPTIONAL)
4A
DEEP P+ (OPTIONAL)

FIG. 3.



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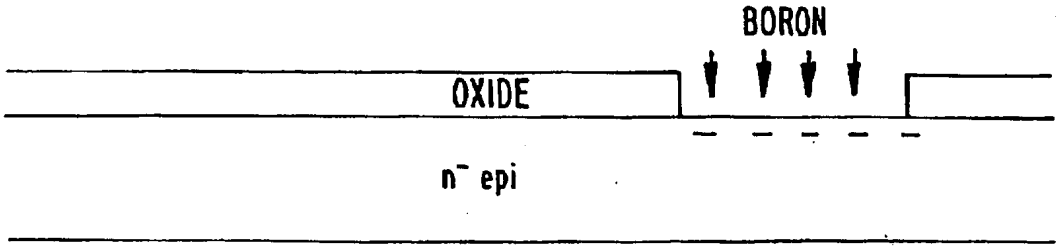
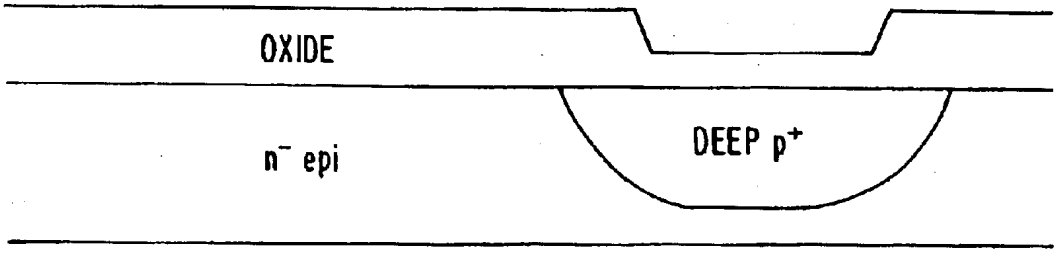


FIG. 4A.



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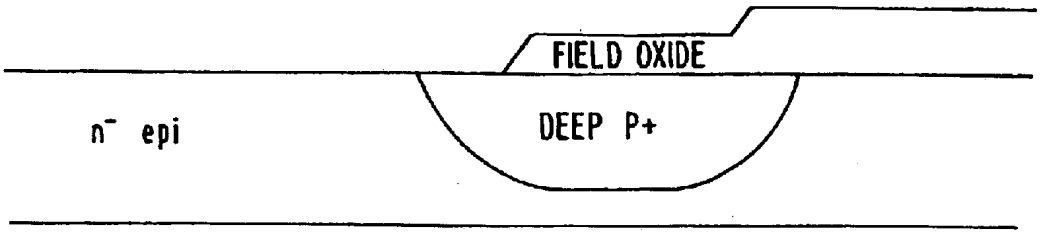

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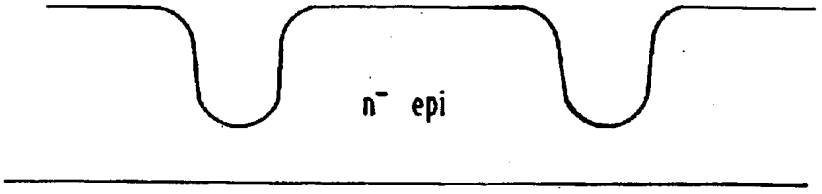

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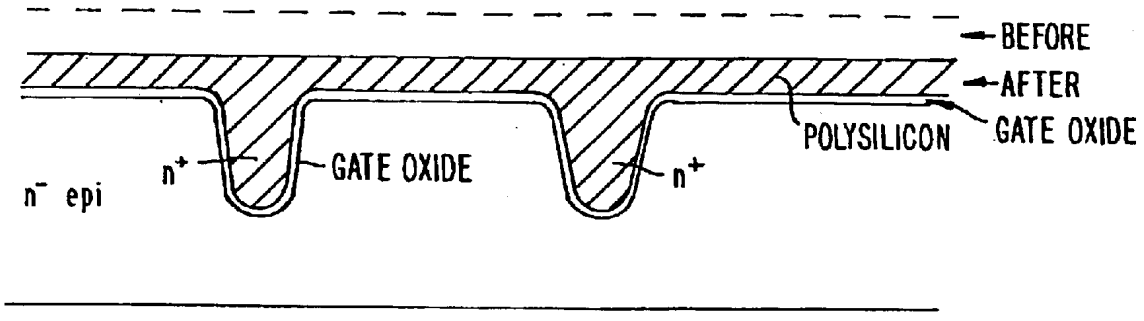

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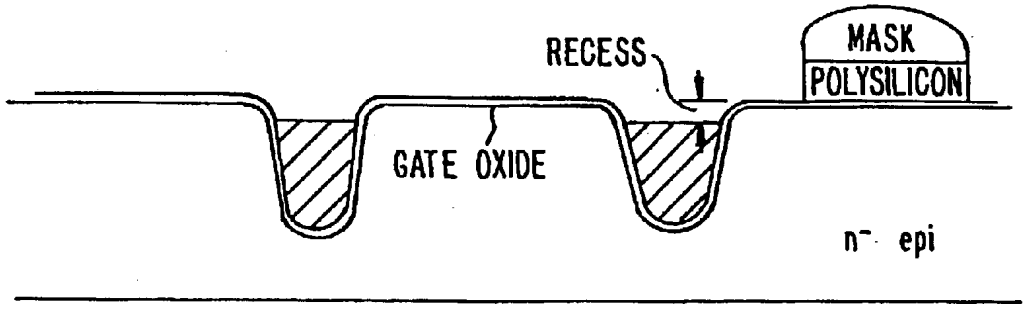

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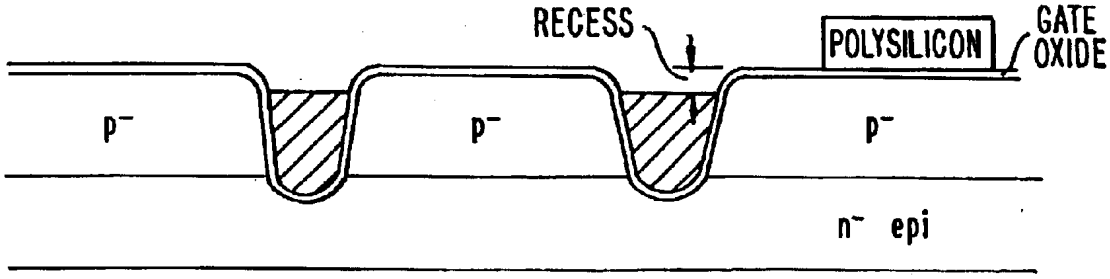

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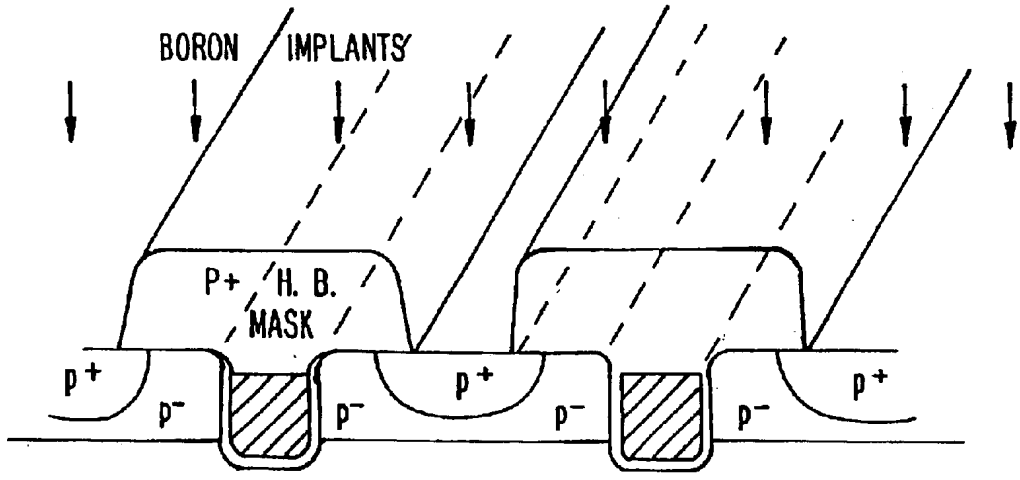

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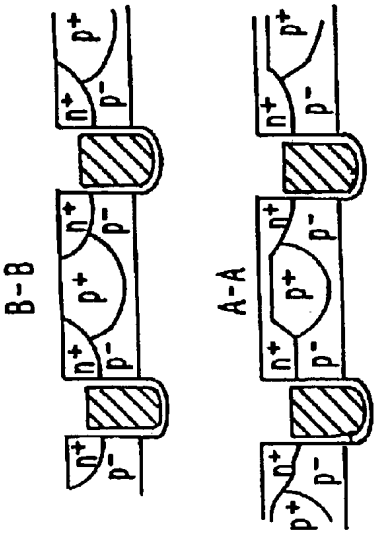


FIG. 4I.

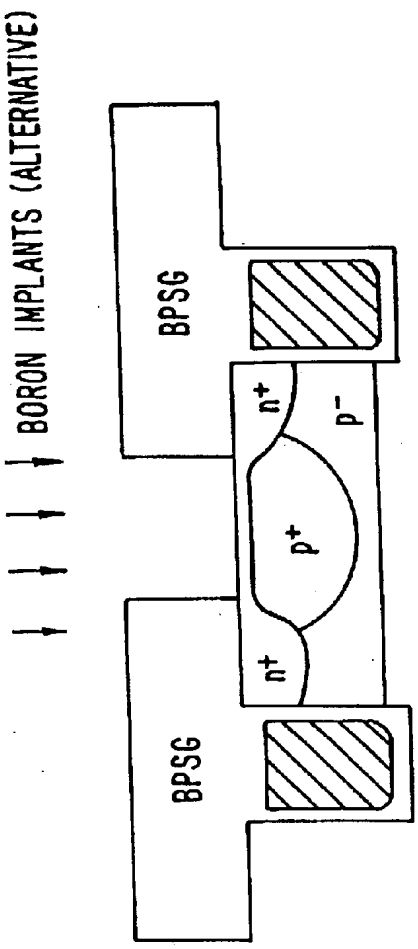
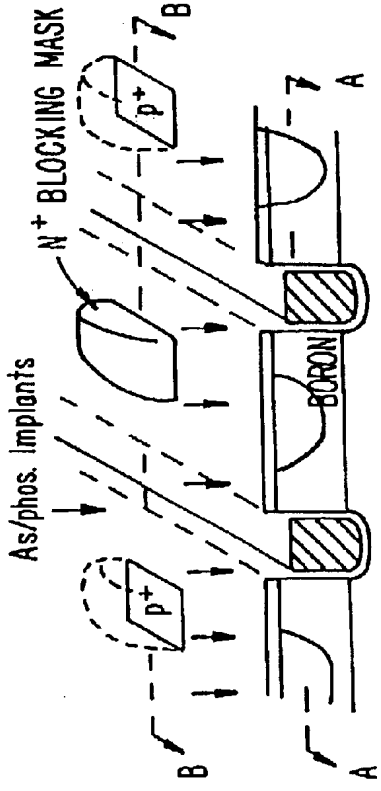


FIG. 4K.



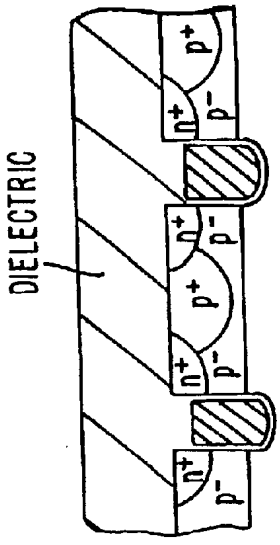
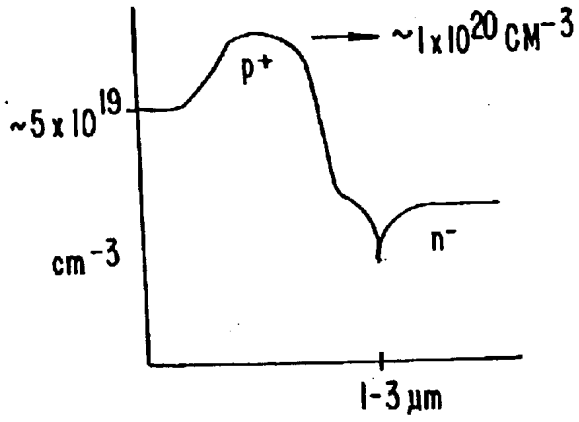


FIG. 4J.



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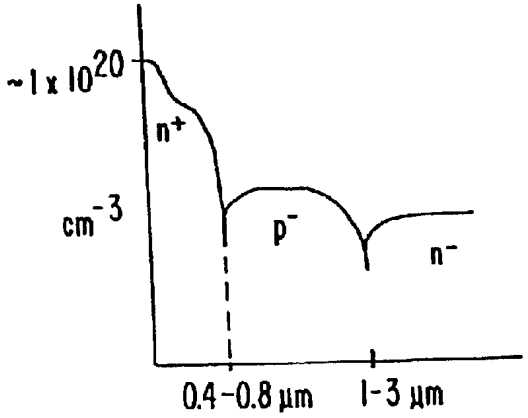

FIG. 5A.

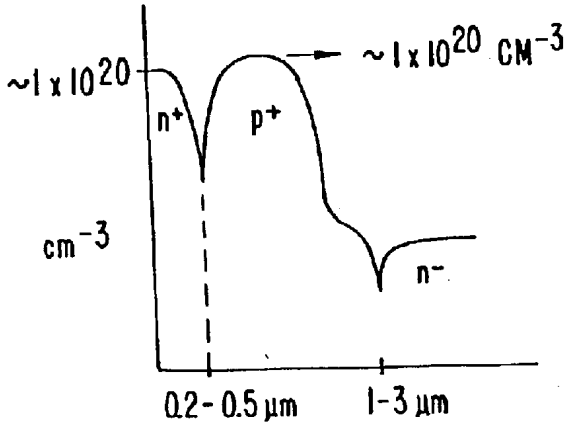

FIG. 5B.

METHOD OF MANUFACTURING A TRENCH TRANSISTOR HAVING A HEAVY BODY REGION

This application is a continuation of and claims the benefit of U.S. application Ser. No. 09/854,102 filed May 9, 2001, now U.S. Pat. No. 6,521,497, which is a divisional of U.S. application Ser. No. 08/970,221 filed Nov. 14, 1997.

BACKGROUND OF THE INVENTION

The present invention relates to field effect transistors, in particular trench DMOS transistors, and methods of their manufacture.

Power field effect transistors, e.g., MOSFETs (metal oxide semiconductor field effect transistors), are well known in the semiconductor industry. One type of MOSFET is a DMOS (double diffused metal oxide semiconductor) transistor. DMOS transistors typically include a substrate on which an epitaxial layer is grown, a doped source junction, a doped heavy body, a doped well of the same (p or n) doping as the heavy body, and a gate electrode. In trenched DMOS transistors the gate electrode is a vertical trench. The heavy body is typically diffused deeper than the bottom of the trench, to minimize electric field at the bottom corners of the trench and thereby prevent avalanche breakdown from damaging the device. The trench is filled with conductive polysilicon, and the polysilicon is generally overetched, to assure that it is completely removed from the surface surrounding the trench. This overetching generally leaves a recess between the top of the polysilicon and the surface of the semiconductor substrate (i.e., the surface of the epitaxial layer). The depth of this recess must be carefully controlled so that it is shallower than the depth of the source junctions. If the recess is deeper than the source junctions the source may miss the gate, resulting in high on-state resistance, high threshold, and potentially a non-functional transistor.

The source and drain junctions can be doped with either p-type or n-type dopants; in either case, the body will be doped with the opposite dopant, e.g., for n-type source and drain the body will be p-type. DMOS transistors in which the source and drain are doped with p-type carriers are referred to as "p-channel". In p-channel DMOS transistors a negative voltage applied to the transistor gate causes current flow from the source region, through a channel region of the body, an accumulation region of the epitaxial layer, and the substrate, to the drain region. Conversely, DMOS transistors, in which the source and drain are doped with n-type carriers, are referred to as "n-channel". In n-channel DMOS transistors a positive voltage applied to the transistor gate causes current to flow from drain to source.

It is desirable that DMOS transistors have low source to drain resistance (Rds_{on}) when turned on and low parasitic capacitance. The transistor structure should also avoid "punchthrough". Punchthrough occurs when, upon application of a high drain to source voltage, depletion into the body region extends to the source region, forming an undesirable conductive path through the body region when the transistor should be off. Finally, the transistor should have good "ruggedness", i.e., a high activation current is needed to turn on the parasitic transistor that inherently exists in DMOS transistors.

Generally a large number of MOSFET cells are connected in parallel forming a single transistor. The cells may be arranged in a "closed cell" configuration, in which the trenches are laid out in a grid pattern and the cells are enclosed on all sides by trench walls. Alternatively, the cells

may be arranged in an "open cell" configuration, in which the trenches are laid out in a "stripe" pattern and the cells are only enclosed on two sides by trench walls. Electric field termination techniques are used to terminate junctions (doped regions) at the periphery (edges) of the silicon die on which the transistors are formed. This tends to cause the breakdown voltage to be higher than it would otherwise be if controlled only by the features of the active transistor cells in the central portions of the die.

SUMMARY OF THE INVENTION

The present invention provides field effect transistors that have an open cell layout that provides good uniformity and high cell density and that is readily scalable. Preferred trenched DMOS transistors exhibit low Rds_{on}, low parasitic capacitance, excellent reliability, resistance to avalanche breakdown degradation, and ruggedness. Preferred devices also include a field termination that enhances resistance to avalanche breakdown. The invention also features a method of making trench DMOS transistors.

In one aspect, the invention features a trenched field effect transistor that includes

(a) a semiconductor substrate, (b) a trench extending a predetermined depth into the semiconductor substrate, (c) a pair of doped source junctions, positioned on opposite sides of the trench, (d) a doped heavy body positioned adjacent each source junction on the opposite side of the source junction from the trench, the deepest portion of the heavy body extending less deeply into said semiconductor substrate than the predetermined depth of the trench, and (e) a doped well surrounding the heavy body beneath the heavy body.

Preferred embodiments include one or more of the following features. The doped well has a substantially flat bottom. The depth of the heavy body region relative to the depths of the well and the trench is selected so that the peak electric field, when voltage is applied to the transistor, will be spaced from the trench. The doped well has a depth less than the predetermined depth of the trench. The trench has rounded top and bottom corners. There is an abrupt junction at the interface between the heavy body and the well, to cause the peak electric field, when voltage is applied to the transistor, to occur in the area of the interface.

In another aspect, the invention features an array of transistor cells. The array includes (a) a semiconductor substrate, (b) a plurality of gate-forming trenches arranged substantially parallel to each other and extending in a first direction, the space between adjacent trenches defining a contact area, each trench extending a predetermined depth into said substrate, the predetermined depth being substantially the same for all of said gate-forming trenches; (c) surrounding each trench, a pair of doped source junctions, positioned on opposite sides of the trench and extending along the length of the trench, (d) positioned between each pair of gate-forming trenches, a doped heavy body positioned adjacent each source junction, the deepest portion of each said heavy body extending less deeply into said semiconductor substrate than said predetermined depth of said trenches, (e) a doped well surrounding each heavy body beneath the heavy body; and (f) p+ and n+ contacts disposed at the surface of the semiconductor substrate and arranged in alternation along the length of the contact area.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15 cm^{-2}. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15 cm^{-2}.

In yet another aspect, the invention features a semiconductor die that includes (a) a plurality of DMOS transistor cells arranged in an array on a semiconductor substrate, each DMOS transistor cell including a gate-forming trench, each of said gate-forming trenches having a predetermined depth, the depth of all of the gate-forming trenches being substantially the same; and (b) surrounding the periphery of the array, a field termination structure that extends into the semiconductor substrate to a depth that is deeper than said predetermined depth of said gate-forming trenches.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5E15 to 1E16 cm^{-2}. The second energy is from about 40 to 70 keV. The second dosage is from about 1E15 to 5E15 cm^{-2}. The resulting depth of the source is from about 0.4 to 0.8 μm the finished DMOS transistor.

The invention also features a method of making a heavy body structure for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into said region a second dopant at a second energy and dosage, said second energy and dosage being relatively less than said first energy and dosage.

Preferred embodiments include one or more of the following features. The first and second dopants both comprise boron. The first energy is from about 150 to 200 keV. The first dosage is from about 1E15 to 5E15. The second energy is from about 20 to 40 keV. The second dosage is from about 1E14 to 1E15.

Additionally, the invention features a method of making a source for a trenched DMOS transistor including (a) providing a semiconductor substrate; (b) implanting into a region of the substrate a first dopant at a first energy and dosage; and (c) subsequently implanting into the region a second dopant at a second energy and dosage, the second energy and dosage being relatively less than the first energy and dosage.

Preferred embodiments include one or more of the following features. The first dopant comprises arsenic and the second dopant comprises phosphorus. The first energy is from about 80 to 120 keV. The first dosage is from about 5E15 to 1E16. The second energy is from about 40 to 70 keV. The second dosage is from about 1E15 to 5E15. The resulting depth of the source is from about 0.4 to 0.8 $_{\mu}$m in the finished DMOS transistor.

In another aspect, the invention features a method of manufacturing a trenched field effect transistor. The method includes (a) forming a field termination junction around the perimeter of a semiconductor substrate, (b) forming an epitaxial layer on the semiconductor substrate, (c) patterning and etching a plurality of trenches into the epitaxial layer; (d) depositing polysilicon to fill the trenches, (e) doping the polysilicon with a dopant of a first type, (f) patterning the substrate and implanting a dopant of a second, opposite type to form a plurality of wells interposed between adjacent trenches, (g)

patterning the substrate and implanting a dopant of the second type to form a plurality of second dopant type contact areas and a plurality of heavy bodies positioned above the wells, each heavy body having an abrupt junction with the corresponding well, (h) patterning the substrate and implanting a dopant of the first type to provide source regions and first dopant type contact areas; and (i) applying a dielectric to the surface of the semiconductor substrate and patterning the dielectric to expose electrical contact areas.

Other features and advantages of the invention will be apparent from the is following detailed description, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a highly enlarged, schematic perspective cross-sectional view showing a portion of a cell array including a plurality of DMOS transistors according to one aspect of the invention. The source metal layer and a portion of the dielectric layer have been omitted to show the underlying layers. FIGS. **1***a* and **1***b* are side cross-sectional views of a single line of transistors from the array of FIG. **1**, taken along lines A—A and B—B, respectively. In FIGS. **1***a* and **1***b* the source metal and dielectric layers are shown.

FIG. **2** is a highly enlarged schematic side cross-sectional view of a semiconductor die showing a portion of the cell array and the field termination.

FIG. **3** is a flow diagram showing the photo mask sequence of a preferred process for forming a trench DMOS transistor of FIG. **1**.

FIGS. **4**–**4***k* are schematic side cross-sectional views showing the individual steps of the process diagrammed in FIG. **3**. The figure numbers for the detailed views in FIGS. **4**–**4***k* are shown parenthetically under the corresponding diagram boxes in FIG. **3**.

FIGS. **5**–**5***b* are spreading resistance profile graphs, reflecting the dopant concentration distribution at different regions of the transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A cell array **10**, including a plurality of rows **12** of trenched DMOS transistors, is shown in FIG. **1**. Cell array **10** has an open cell configuration, i.e., trenches **14** run in only one direction, rather than forming a grid. Individual cells are formed by alternating n+ source contacts **16** and p+ contacts **18** in rows **20** that run parallel to and between trenches **14**. The configuration of the regions of each row that have an n+ source contact are shown in cross-section in FIG. **1***a*, while the regions that have a p+ contact are shown in FIG. **1***b*.

As shown in FIGS. **1***a* and **1***b*, each trenched DMOS transistor includes a doped n+ substrate (drain) layer **22**, a more lightly doped n− epitaxial layer **24**, and a gate electrode **28**. Gate electrode **28** comprises a conductive polysilicon that fills a trench **14**. A gate oxide **26** coats the walls of the trench and underlies the polysilicon. The top surface of the polysilicon is recessed from the surface **30** of the semiconductor substrate by a distance R (typically from about 0 to 0.4 μm). N+ doped source regions **32***a*, **32***b* are positioned one on each side of the trench **14**. A dielectric layer **35** covers the trench opening and the two source regions **32***a*, **32***b*. Extending between the source regions of adjacent cells is a p+ heavy body region **34** and, beneath it, a flat-bottomed p− well **36**. In the areas of the cell array which have a n+ contact **16**, a shallow n+ doped contact region extends between the n+ source regions. A source metal layer **38** covers the surface of the cell array.

The transistor shown in FIGS. **1***a* and **1***b* includes several features that enhance the ruggedness of the transistor and its resistance to avalanche breakdown degradation.

First, the depth of the p+ heavy body region **34** relative to the depths of the trench **14** and the flat bottom of the p− well

is selected so that the peak electric field when voltage is applied to the transistor will be approximately halfway between adjacent trenches. The preferred relative depths of the p+ heavy body, the p− well and the trench are different for different device layouts. However, preferred relative depths can be readily determined empirically (by observing the location of peak electric field) or by finite element analysis.

Second, the bottom corners of the trench **14** are rounded (preferably, the top corners are also rounded; this feature is not shown). Corner rounding can be achieved using the process described in U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635. The rounded corners of the trench also tend to cause the peak electric field to be moved away from the trench corners and towards a central location between adjacent trenches.

Third, an abrupt junction at the interface between the p+ heavy body and the p− well causes the peak electric field to occur in that area of the interface. Avalanche multiplication initiates at the location of the peak electric field, thus steering hot carriers away from the sensitive gate oxide and channel regions. As a result, this structure improves reliability and avalanche ruggedness without sacrificing cell density as much as a deeper heavy body junction. This abrupt junction can be achieved by the double doping process that will be described below, or by other processes for forming abrupt junctions, many of which are known in the semiconductor field.

Lastly, referring to FIG. **2**, the cell array is surrounded by a field termination junction **40** which increases the breakdown voltage of the device and draws avalanche current away from the cell array to the periphery of the die. Field termination junction **40** is a deep p+ well, preferably from about 1 to 3 μm deep at its deepest point, that is deeper than the p+ heavy body regions **34** in order to reduce the electric field caused by the junction curvature. A preferred process for making the above-described transistors is shown as a flow diagram in FIG. **3**, and the individual steps are shown schematically in FIGS. **4**–**4***k*. It is noted that some steps that are conventional or do not require illustration are described below but not shown in FIGS. **4**–**4***k*. As indicated by the arrows in FIG. **3**, and as will be discussed below, the order of the steps shown in FIGS. **4**–**4***k* can be varied. Moreover, some of the steps shown in FIGS. **4**–**4***k* are optional, as will be discussed.

A semiconductor substrate is initially provided. Preferably, the substrate is a N++ Si substrate, having a standard thickness, e.g., 500 μm, and a very low resistivity, e.g., 0.001 to 0.005 Ohm-cm. An epitaxial layer is deposited onto this substrate, as is well known, preferably to a thickness of from about 4 to 10 μm. Preferably the resistivity of the epitaxial layer is from about 0.1 to 3.0 Ohm-cm.

Next, the field termination junction **40** is formed by the steps shown in FIGS. **4**–**4***c*. In FIG. **4**, an oxide layer is formed on the surface of the epitaxial layer. Preferably, the thickness of the oxide is from about 5 to 10 kÅ. Next, as shown in FIG. **4***a*, the oxide layer is patterned and etched to define a mask, and the p+ dopant is introduced to form the deep p+ well field termination. A suitable dopant is boron, implanted at an energy of from about 40 to 100 keV and a dose of 1E14 (1×10^{14}) to 1E16 cm^{-2}. As shown in FIG. **4***b*, the p+ dopant is then driven further into the substrate, e.g., by diffusion, and a field oxide layer is formed over the p+ junction. Preferably the oxide thickness is from about 4 to 10 kÅ. Finally, the oxide (FIG. **4**) over the active area of the substrate (the area where the cell array will be formed) is patterned and removed by any suitable etching process, leaving only the field oxide in suitable areas. This leaves the substrate ready for the following steps that will form the cell array.

It is noted that, as an alternative to steps **4**–**4***c*, a suitable field termination structure can be formed using a ring-shaped trench which surrounds the periphery of the cell array and acts to lessen the electric field and increase the resistance to avalanche breakdown degradation. This trench field termination does not require a field oxide or deep p+ body junction to be effective. Consequently, it can be used to reduce the number of process steps. Using a trench ring (or multiple concentric trench rings) to form a field termination is described in, e.g., U.S. Pat. No. 5,430,324, the full disclosure of which is hereby incorporated herein by reference. Preferably, the trench would have substantially the same depth as the trenches in the cell array.

The cell array is formed by the steps shown in FIGS. **4***d*–**4***k*. First, a plurality of trenches are patterned and etched into the epitaxial layer of the substrate (FIG. **4***d*). Preferably, as noted above, the trenches are formed using the process U.S. application Ser. No. 08/959,197, filed on Oct. 28, 1997, now U.S. Pat. No. 6,103,635, so that the upper and lower corners of each trench will be smoothly rounded. As shown in FIG. **1** and described above, the trenches are patterned to run in only one direction, defined as an open cell structure. After trench formation, a gate oxide layer is formed on the trench walls, as is well known in the semiconductor field. Preferably the gate oxide has a thickness of from about 100 to 800 Å.

Next, as shown in FIG. **4***e*, polysilicon is deposited to fill the trench and cover the surface of the substrate, generally to a thickness of from about 1 to 2 μm depending on the trench width (shown by the dotted lines in FIG. **4***e*). This layer is then planarized by the nature of its thickness relative to the trench width, typically from about 2 to 5 kÅ (indicated by solid lines in FIG. **4***e*). The polysilicon is then doped to n-type, e.g., by conventional $POCL_3$ doping or by phosphorus implant. The backside of the wafer need not be stripped (as is conventionally done prior to doping the polysilicon to enhance defect gettering) because any further doping of the highly doped substrate would be unlikely to result in any enhancement in defect gettering.

The polysilicon is then patterned with a photoresist mask and etched to remove it from the trench areas, as shown in FIG. **4***f*. A small recess between the top of the polysilicon in the trench and the substrate surface inherently results when the polysilicon is etched completely to remove all of the polysilicon from the substrate surface. The depth of this recess must be controlled so that it does not exceed the depth of the n+ source junction that will be formed in a later step. To reduce the need to carefully control this aspect of the process, a relatively deep n+ source junction is formed, as will be discussed below.

Then, as shown in FIG. **4***g*, the p− well is formed by implanting the dopant, e.g., a boron implant at an energy of 30 to 100 keV and a dosage of 1E13 to 1E15, and driving it in to a depth of from about 1 to 3 μm using conventional drive in techniques.

The next two steps (p+ heavy body formation) can be performed either before formation of the n+ source junction, or afterwards, as indicated by the arrows in FIG. **3**. P+ heavy body formation and n+ source junction formation can be performed in either order because they are both resist-masked steps and because there is no diffusion step in between. This advantageously allows significant process

flexibility. The p+ heavy body formation steps will be described below as being performed prior to source formation; it will be understood that n+ source formation could be performed first simply by changing the order of the steps discussed below.

First, a mask is formed over the areas that will not be doped to p+, as shown in FIG. **4***h*. (It is noted that this masking step is not required if the p+ heavy body is formed later, after the dielectric layer has been applied and patterned for contact holes. (see FIG. **4***k*, below) so that the dielectric itself provides a mask.) As discussed above, it is preferred that the junction at the interface between the p− well and the p+ heavy body be abrupt. To accomplish this, a double implant of dopant (e.g., boron) is performed. For example, a preferred double implant is a first boron implant at an energy of 150 to 200 keV and a dose of 1E15 to 5E15 cm^{-2}, and a second boron implant at an energy of 20 to 40 keV and a dose of 1E14 to 1E15 cm^{-2}. The high energy first implant brings the p+ heavy body as deep as possible into the substrate, so that it will not compensate the n+ source junction to be introduced later. The second, lower energy/lower dose implant extends the p+ heavy body from the deep region formed during the first implant up to the substrate surface to provide the p+ contact **18**. The resulting p+ heavy body junction is preferably about 0.4 to 1 μm deep at this stage of the process (final junction depth after drive-in is preferably about 0.5 to 1.5 μm deep), and includes a region of high dopant concentration near the interface with the p− well, and a region of relatively low dopant concentration at the contact surface of the p+ heavy body. A preferred concentration distribution is shown in FIG. **5**.

It will be appreciated by those skilled in the art that the abrupt junction can be formed in many other ways, e.g., by diffused dopants, by using a continuous dopant source at the surface or by using atoms that diffuse slowly.

After the formation of the p+ heavy body, a conventional resist strip process is performed to remove the mask, and a new mask is patterned to prepare the substrate for the formation of the n+ source junction. This mask is a n+ blocking mask and is patterned to cover the areas of the substrate surface which are to provide p+ contacts **18** (FIGS. **1** and **1***b*), as shown in FIG. **4***i*. This results in the formation of alternating p+ and n+ contacts after n-type doping (see lines A—A and B—B and cross-sectional views A—A and B—B in FIG. **4**I, which correspond to FIGS. **1***a* and **1***b*).

The n+ source regions and n+ contact are then formed using a double implant. For example, a preferred double implant process is a first implant of arsenic at an energy of 80 to 120 keV and a dose of 5E15 to 1E16 cm^{-2} followed by a second implant of phosphorus at an energy of 40 to 70 keV and a dose of 1E15 to 5E15 cm^{-2}. The phosphorus implant forms a relatively deep n+ source junction, which allows more process flexibility in the depth of the polysilicon recess, as discussed above. Phosphorus ions will penetrate deeper into the substrate during implant and also during later diffusion steps. Advantageously, the n+ source regions will have a depth of about 0.4 to 0.8 μm after diffusion. The arsenic implant extends the n+ source to the substrate surface, and also forms the n+ contacts **16** (see FIGS. **1** and **1***a*) by compensating (converting) the p-type surface of the p+ heavy body to n-type in the desired contact area. The preferred sheet resistance profiles for the n+ source along the edge of the trench, and the n+ contact are shown in FIGS. **5***a* and **5***b*, respectively.

Thus, the alternating p+ and n+ contacts **18**, **16**, shown in FIG. **1** are formed by patterning the substrate with appropriate masks and doping with the first p+ implant and the second n+ implant, respectively, as described above. This manner of forming the alternating contacts advantageously allows an open cell array having a smaller cell pitch than is typical for such arrays and thus a higher cell density and lower Rds_{on}.

Next, a conventional n+ drive is performed to activate the dopants. A short cycle is used, preferably 10 min at 900° C., so that activation occurs without excessive diffusion.

A dielectric material, e.g., borophosphate silicate glass (BPSG), is then deposited over the entire substrate surface and flowed in a conventional manner (FIG. **4***j*), after which the dielectric is patterned and etched (FIG. **4***k*) to define electrical contact openings over the n+ and p+ contacts **16**, **18**.

As noted above, the p+ heavy body implant steps can be performed at this point, if desired (rather than prior to n+ source formation), eliminating the need for a mask and thus reducing cost and process time.

Next, the dielectric is reflowed in an inert gas, e.g., a nitrogen purge. If the p+ body has been implanted immediately prior, this step is required to activate the p+ dopant. If the p+ body was implanted earlier, prior to the n+ drive, this step can be omitted if the dielectric surface is sufficiently smooth-edged around the contact openings.

The cell array is then completed by conventional metalization, passivation deposition and alloy steps, as is well know in the semiconductor field.

Other embodiments are within the claims. For example, while the description above is of an n-channel transistor, the processes of the invention could also be used to form a p-channel transistor. To accomplish this, "p" and "n" would simply be reversed in the above description, i.e., where "p" doping is specified above the region would be "n" doped instead, and vice versa.

What is claimed is:

1. A method of manufacturing a trench transistor comprising:

providing a semiconductor substrate having dopants of a first conductivity type;

forming a plurality of trenches extending to a first depth into the semiconductor substrate;

lining each of the plurality of trenches with a gate dielectric material;

substantially filling each dielectric-lined trench with conductive material;

forming a doped well in the substrate to a second depth that is less than said first depth of the plurality of trenches, the doped well having dopants of a second conductivity type opposite to said first conductivity type;

forming a heavy body extending inside the doped well to a third depth that is less than said second depth of said doped well, the heavy body having dopants of the second conductivity type and forming an abrupt junction with the well; and

forming a source region inside the well, the source region having dopants of the first conductivity types.

2. The method of claim **1** wherein the step of forming a doped well forms the well with a substantially flat bottom.

3. The method of claim **1** further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

4. The method of claim **3** wherein the step of forming a deep doped region forms a PN junction diode with the substrate that helps improve a breakdown voltage of the transistor.

5. The method of claim **3** wherein the deep doped region forms a termination structure around the periphery of the substrate.

6. The method of claim **1** wherein the step of substantially filling each dielectric-lined trench leaves a recess at an upper portion of each trench.

7. The method of claim **6** further comprising filling the recess at the upper portion of each trench with dielectric material.

8. The method of claim **1** wherein the step of forming the heavy body comprises a double implant process.

9. The method of claim **8** wherein the double implant process comprises:

a first implant of dopants of the first conductivity type, at a first energy level and a first dosage to form a first doped portion of the heavy body; and

a second implant of dopants of the first conductivity type, at a second energy level and a second dosage to form a second doped portion of the heavy body.

10. The method of claim **9** wherein the first implant occurs at approximately the third depth.

11. The method of claim **9** wherein the first energy level is higher than the second energy level.

12. The method of claim **11** wherein the first dosage is higher than the second dosage.

13. The method of claim **1** wherein the step of forming the heavy body comprises a process of diffusing dopants of the second conductivity type.

14. The method of claim **1** wherein the step of forming the heavy body comprises using a continuous dopant source at the surface of the semiconductor substrate.

15. The method of claim **1** wherein the step of forming a plurality of trenches comprises patterning and etching the plurality of trenches that extend in parallel along a longitudinal axis.

16. The method of claim **15** further comprising forming a contact area on the surface of the substrate between adjacent trenches.

17. The method of claim **16** wherein the step of forming the contact area comprises forming alternating source contact regions and heavy body contact regions.

18. The method of claim **16** wherein the step of forming the contact area comprises forming a ladder-shaped source contact region surrounding heavy body contact regions.

19. The method claim **18** wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises:

forming a source blocking mask on the surface of the semiconductor substrate patterned to cover the heavy body contact regions; and

implanting dopants of the first conductivity type to form the ladder-shaped source contact region.

20. The method of claim **18** wherein the step of forming the ladder-shaped source contact region surrounding heavy body contact regions, comprises forming a dielectric layer on the surface of the semiconductor substrate patterned to expose the heavy body contact regions.

21. A method of manufacturing a trench field effect transistor on a semiconductor substrate having dopants of a first conductivity type, the method comprising:

etching a plurality of trenches into the semiconductor substrate to a first depth;

lining the plurality of trenches with dielectric layer;

substantially filling the dielectric-lined plurality of trenches with conductive material;

forming a well between adjacent trenches to a second depth that is shallower than the first depth, the well having dopants of second conductivity type opposite to the first conductivity type;

forming a heavy body inside the well to a third depth that is shallower than the second depth, the heavy body having dopants of the second conductivity type; and

forming a source region inside the well and adjacent to trenches, the source region having dopants of the first conductivity type,

wherein, the step of forming a heavy body employs a process to form an abrupt junction between the heavy body and the well at approximately the third depth.

22. The method of claim **21** further comprising adjusting a location of the abrupt junction relative to the depth of the well so that a transistor breakdown current is spaced away from the trench in the semiconductor.

23. The method of claim **21** further comprising forming a deep doped region having dopants of the second conductivity type, the deep doped region extending into the substrate to a fourth depth that is deeper than said first depth of the trench.

* * * * *

EXHIBIT 5

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September 12, 2007

VIA ELECTRONIC MAIL AND U.S. MAIL

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Re: Alpha & Omega Semiconductor, Ltd. v. Fairchild Semiconductor Corp.,
Case No. C 07-2638 JSW (consolidated with Case No. C-07-2664 JSW)
Our File No.: 18865P-021600

Dear Brett:

This letter concerns AOS's Disclosure of Asserted Claims and Preliminary Infringement Contentions Pursuant to Patent L.R. 3-1 ("PICs") served on August 31, 2007.

AOS's PICs fail to provide the required disclosure under Patent L.R. 3-1. The overriding principle of the Patent Local Rules is to streamline the discovery process and make it more efficient by requiring a plaintiff to articulate its claims with specificity. *See Intertrust Technologies Corp. v. Microsoft Corp.*, 2003 WL 23120174, *1 (N.D. Cal. 2003). The intent of the rule is to "require parties to crystallize their theories of the case early in the litigation" and to adhere to those theories once they have been disclosed. *Id.* (citation omitted); *O2 Micro Intern. Ltd. v. Monolithic Power Sys, Inc.*, 467 F.3d 1355, 1364 (Fed. Cir. 2006) (citation omitted). AOS's PICs fail to provide the required disclosure in at least the following ways.

First, Patent L.R. 3-1(c) requires AOS to provide a chart "identifying specifically where each element of each asserted claim is found within each Accused Instrumentality." AOS's PICs are completely devoid of any specific information identifying anything in the accused products or methods that allegedly practices the elements of the asserted claims. AOS's entire disclosure appears to consist merely of parroting back the language of each claim element with an accompanying assertion that Fairchild's accused methods or products include that claim element, without any supporting analysis or evidence. For example, below is the disclosure for the claim element identified by AOS as element (b) of claim 1 of U.S. Patent No. 5,907,776 ("the 776 Patent"):

(b) forming at least one trench in said substrate;	The Accused '776 Patent Methods include the step of forming at least one trench gate in the aforementioned substrate.

AOS has merely taken the language of the claim element from the first column ("forming at least one trench in said substrate"), parroted it back in the second column (". . . the step of forming at least one trench gate in the aforementioned substrate") and included introductory language that asserts without any basis that the accused methods include this step. This disclosure does not provide sufficient information to articulate AOS's claims or theories of infringement as required by the Northern District of California Patent Local Rules or case law. *See Intertrust,* 2003 WL 23120174, *1; *O2 Micro*, 467 F.3d at 1364.

AOS follows the same formula for the other claim elements of the '776 Patent. For example, below is the disclosure for the claim element identified by AOS as element (d) of claim 13 of the '776 Patent:

(d) compensating a portion of said body region by implanting material of said second conductivity type in said body region	The Accused '776 Patent Methods include the step of compensating a portion of the aforementioned body region. This step includes at least implanting dopants of the same conductivity type as the aforementioned source region.

The disclosure for the only asserted claim of U.S. Patent No. 5,767,567 ("the "567 Patent) is similarly devoid of any substance. For example, below is the disclosure for the claim element identified by AOS as element (b) of claim 7 of the '567 Patent:

(b) configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios for disposing several of said lead wires in each of said sub-contact areas according to said set of area proportional ratios.	The Accused '567 Patent Methods include the step of dividing the source contact area with the one or more gate runners into two or more subsections. The subsections of the source contact area are divided so that they are of proportional ratios for disposing the lead wires in accordance with the ratios.

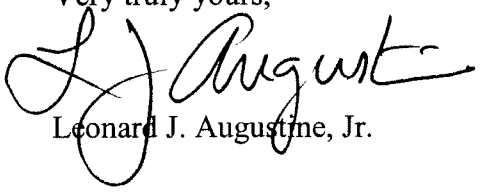
This disclosure also does not provide sufficient information to articulate AOS's claims or theories of infringement as required by the Northern District of California Patent Local Rules or case law. *See Intertrust,* 2003 WL 23120174, *1; *O2 Micro*, 467 F.3d at 1364.

Finally, Patent L.R. 3-1(f) requires that AOS identify "separately for each asserted claim," each AOS apparatus, produce, device, method, act, or other instrumentality that incorporates or reflects "that particular claim." AOS has provided in Exhibit C a list of AOS products that it alleges practice the claimed inventions, but did not identify *which* AOS products are alleged to practice *which* asserted claims.

Rule 11 of the Federal Rules of Civil Procedure requires a party to conduct a reasonable inquiry into the applicable facts and law before filing a document, to include "investigat[ing] the factual and legal basis for the complaint before filing suit." *Network Caching Technology, LLC v. Novell, Inc.*, 2002 WL 32126128, *4 (N.D. Cal.) (granting in part motion to strike PICs). In applying Rule 11 to Patent L.R. 3-1, "a plaintiff must put forth information so specific that either reverse engineering or its equivalent is required." *Intertrust*, 2003 WL 23120174, *2. AOS's PICs clearly fall short of the required disclosure.

Please provide amended PICs that comply with the requirements of the Patent Local Rules within the next seven days. Fairchild's Preliminary Invalidity Contentions are due within 45 days of service of AOS's Preliminary Infringement Contentions, and we interpret that to mean service of contentions that comply with the Patent Local Rules.

Very truly yours,



Leonard J. Augustine, Jr.

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EXHIBIT 6

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September 21, 2007

VIA E-MAIL AND U.S. MAIL

Leonard J. Augustine, Jr.
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Re: *Alpha & Omega Semiconductor, Ltd. et al. v. Fairchild Semiconductor Corp.*, Case No. C 07-2638 JSW (consolidated with Case No. C 07-2664 JSW)

Dear Mr. Augustine:

I write in response to your letter to Brett Schuman dated September 12, 2007 regarding AOS's Disclosure of Asserted Claims and Preliminary Infringement Contentions ("PICs"). We disagree with your contentions regarding AOS's PICs, and we have a number of issues with Fairchild's Patent L.R. 3-1 Disclosures.

In your letter, you contend that "AOS's PICs are completely devoid of any *specific information* identifying anything in the accused products or methods that allegedly practices the elements of the asserted claims." (emphasis added). We disagree. Significantly, AOS has identified specific Fairchild products—by part number—that are believed to be manufactured using methods disclosed by the asserted patents. Furthermore, for each of the methods that are believed to be used in the manufacture of these products, AOS has provided a chart identifying—on an element-by-element basis—where in the accused products or processes the claim elements are found. In some instances, the description of the step happens to coincide with the claim language in large part because that is the language that describes the step, *e.g.*, "providing a substrate" or "forming a trench."

Indeed, AOS's disclosures use very similar language to the language Fairchild used in its own PICs. For example, Fairchild's PICs include the following language (Exhibit 30):

forming a plurality of trenches extending to a first depth into the semiconductor substrate;	The accused method includes creating a plurality of trenches that extend to a predetermined depth into the substrate (a first depth). (Fig. AO4812-3 (Scanning Electron Microscopy image), item B; Fig. AO4812-4 (Scanning Capacitance Microscopy image), item B.)

This disclosure parallels the AOS disclosure you identify as faulty in your letter:

(b) forming at least one trench in said substrate;	The Accused '776 Patent Methods include the step of forming at least one trench gate in the aforementioned substrate.

In light of the similarities between the parties' disclosures, it is difficult for AOS to understand the issues Fairchild has raised with respect to AOS' claims charts.

Moreover, as noted in AOS's PICs, AOS provided the PICs prior to receiving any discovery for Fairchild. Accordingly, AOS cannot be expected to identify at this stage of the litigation the steps or elements of Fairchild's processes using the specific language that Fairchild uses to refer to those steps, or to correlate the claim elements to the steps as described in Fairchild's processing recipes or other documents.

Fairchild's own PICs include far more significant flaws, and fail to comply with Patent L.R. 3-1. For example, Fairchild's identification of the AOS products that Fairchild accuses of infringement does not appear to be a good faith identification complying with the appropriate rules. Fairchild states that every product listed in AOS's "all products" selection guide infringes every accused Fairchild claim. This "shotgun" identification is starkly inconsistent with the statement in your letter that "the overriding principle of the Patent Local Rules is to streamline the discovery process," and is particularly improper given that Fairchild only provides claim charts for a handful of products, with no suggestion of how those charts justify assertions that every other AOS product infringes. Further, in its pre-litigation correspondence, Fairchild only identified certain AOS products. Fairchild must limit its accusation to those products that it in good faith believes infringe its patents.

Also, with respect to Fairchild's disclosure under Patent L.R. 3-1(f), Fairchild has not identified specific products that practice the asserted claims, but simply states "PowerTrench MOSFETS." Fairchild must amend its Patent L.R. 3-1(f) disclosure to identify specific products, and not just categories of products, that reflect each of the asserted claims.

Finally, the exhibits to Fairchild's Patent L.R. 3-1 Disclosures are also improper. Fairchild includes various analyses purportedly supporting the accusations of its claim charts, including SEMs, SCMs, and SIMS analyses. Fairchild, however provides no information or

documentation regarding these purported analyses, including documents explaining what products were analyzed, the parameters of the analyses, how the images were generated, etc. For example, it is not clear if the SIMS images are taken from a single analysis or are created from a compilation of analyses, nor is it even clear what part of the device is being analyzed. Even more strikingly, for some of the products, Fairchild provides analysis for a product, and then acknowledges that the analysis is actually of a different product. Further, we suspect that at least one of the parts identified is not even an AOS product.

Indeed, we invite you to review the analyses included in Fairchild's Patent L.R. 3-1 disclosures and confirm that you believe the products infringe, since it appears that some of the products do not infringe even under what we suspect is Fairchild's theory of infringement.

Please let me know your thoughts on these matters. Thank you.

Sincerely,

Andrew J. Wu for/by permission